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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,155	10/25/2001	Sailesh Kottapalli	42P12494	7078

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,155	KOTTAPALLI ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *14-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the applicant's RCE dated 7/7/2005 and amendment dated 11/21/2005.

The applicant has withdrawn Claims 14-17 from consideration.

The applicant has amended Claim 1.

Claims 1-13 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/21/2005 has been entered.

Response to Amendment

2. As per Cohen Art Argument:

The applicant's arguments for Claims 1-9 are moot in view of the applicant's amendment in regard to Claim1, and new rejections under 35 USC 103 (see below).

3. As per 35 USC 103 Rejections:

The applicant has not presented an argument for Claims 10-13, and thus the rejections of said claims are maintained. Applicant should submit an argument under the heading "Remarks" pointing out disagreements with the examiner's contentions. Applicant must also discuss the references applied against the claims, explaining how the claims avoid the references or distinguish from them (see MPEP 714.03 ¶ 7.95.01 Lack of Arguments in Response).

Claim Rejections - 35 USC § 103(New)

4. Claims 1, 2, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, "The Cache Memory Book", and further in view of McClure, U.S. Patent No. 5666482.

As per Claim 1:

Handy teaches an apparatus comprising: a processor coupled to a set associative cache memory (page 58, FIG. 2.11); the set-associative cache memory with a plurality of ways (FIG. 2.12), each way with a plurality of cache lines (page 146 FIG. 4.7), each cache line with at least one valid bit to indicate whether the line is valid (page 51-59 and FIG. 2.8). But Handy fails to disclose a "faulty status" bit. But in the analogous art of McClure, such a feature is taught, wherein there is at least one status bit to represent whether the cache line contains a defect (column 8 lines 59-61); and a logic to perform at least one test of the plurality of cache lines and to set the status bit for at least one of the plurality of cache lines (column 8 lines 53-61). And McClure, in column 3 lines 57-67 and column 4 lines 1-10, recites the advantage being a cache

memory system that utilizes a "faulty status" bit in order to compensate for bad memory locations in a set-associative cache memory. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to include the faulty status bit capabilities as well as test capacity of McClure to the cache memory of Handy in order to save the expense of replacing a logic device because of a bad data line.

As per Claim 2:

McClure further teaches the apparatus of claim 1 wherein the logic is a programmable built in self-test (PBIST) logic (column 10 lines 3-4). And in view of the motivation previously stated, the claim is rejected.

As per Claim 5:

McClure further teaches the apparatus of claim 1 wherein the status bit is stored in a register file cell (column 10 lines 1-2). And in view of the motivation previously stated, the claim is rejected.

As per Claim 8:

McClure further teaches the apparatus of claim 1 wherein the cache memory is either one of a level 0 (L0) cache, level 1 (L1) cache, or level 2 (L2) cache (column 10 lines 22-23 and column 2 lines 29-36). And in view of the motivation previously stated, the claim is rejected.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, "The Cache Memory Book", and further in view of McClure, U.S. Patent No. 5666482 as

applied to Claim 1, and further in view of Crouch et al., U.S. Patent No. 5592493. McClure further teaches the apparatus of claim 1 wherein the logic is a plurality of scan chains (column 10 lines 1-2), but does not teach a test access port to accept automatic test pattern generation (ATPG) patterns. But in an analogous art, Crouch et al. tests a cache (column 7 lines 5-10) using a test access port (column 2 lines 5-13), using ATPG patterns (column 2 lines 51-65). It would have been obvious to modify the apparatus of McClure by providing a TAP such as the one taught by Crouch et al. in order to utilize ATPG patterns. And Crouch et al., in column 1 lines 10-30, recites a need to efficiently test and to access components such as a cache by using this invention. One with ordinary skill in the art at the time of the invention, motivated by Crouch et al., would combine the references to use ATPG in testing a cache, and so the claim is rejected.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, "The Cache Memory Book", and further in view of McClure, U.S. Patent No. 5666482 as applied to Claim 1, and further in view of the applicant's admitted prior art. McClure further teaches the apparatus of claim 1 wherein the status bit is stored in a six-transistor static random access memory cell (column 10 lines 5-6). The examiner notes that it is well known in the art that a non-volatile device is an SRAM device, and a six-transistor SRAM device is admitted prior art for an SRAM as admitted to by the applicant (Application, page 5 line 19). And in view of the motivation previously stated, the claim is rejected.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, "The Cache Memory Book", and further in view of McClure, U.S. Patent No. 5666482 as applied to Claim 1, and further in view of Aipperspach et al., U.S. Patent No. 6181614. McClure teaches the apparatus of claim 1 but does not specifically teach wherein the status bit is stored in a fuse. In analogous art, Aipperspach et al. does teach this feature in column 2 lines 21-22. It would have been obvious to modify the circuit of McClure to include permanently modifiable cells of a fusible type to make changes permanent. And in column 2 lines 1-20 the inventor describes the advantage of a self-repair system using persistent repair information. One with ordinary skill in the art at the time of the invention, motivated by Aipperspach et al., would combine the references, and so the claim is rejected.

8. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handy, "The Cache Memory Book", and further in view of McClure, U.S. Patent No. 5666482 as applied to Claim 1, and further in view of Phan, U.S. Patent No. 6634003. As per Claim 7:

McClure teaches the apparatus of claim 1 but is not specific in teaching that the status bit is a read only bit during normal operation of the system. In an analogous art, Phan does teach this feature. The status bit (FIG.4) is activated only during test and initialization (column 6 lines 8-65), and therefore is read only in normal operation (column 4 lines 11-24). It would have been obvious to make the replacement circuits non-modifiable during normal operation as taught by Phan. And Phan, in column 1 lines

47-61 recites need to improve circuit speed by using the status bit instead of address compares for fault indication during normal operation of a cache. And one with ordinary skill in the art at the time of the invention, motivated as suggested by Phan, would combine the references to improve cache access speed, and thus the claim is rejected. As per Claim 9:

McClure teaches the apparatus of claim 2, and Phan teaches wherein the PBIST logic can set the status bit during initialization of the cache memory (column 6 lines 8-65). And in view of the obviousness and motivation already recited, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

ALBERT DECADY